DIGITAL CORRELATED DOUBLE SAMPLING USING DUAL ANALOG PATH

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BACKGROUND

[0001]   One differentiating feature of imaging sensors such as CCD and CMOS image sensors is the image quality generated under low light conditions. To produce a high quality image under low light conditions, imaging sensors generally need to eliminate as much noise as possible. One way to reduce noise is correlated double sampling (CDS). CDS generates a corrected pixel value by finding the difference between a raw integrated signal for an exposed pixel and a reset signal for the pixel. Subtracting the actual dark or reset output level of a pixel sensor from the actual light-induced signal of the pixel sensor effectively removes static fixed pattern noise and several types of temporal noise.

[0002]   The subtraction of signals CDS can be done either in the analog or digital domain. Analog CDS generally requires large capacitors to sample and hold the reset voltage during the exposure time. These capacitors may be subject to leakage particularly for long exposure times. In contrast, digital CDS can store digital reset values in RAM, which is not subject to data degradation during the exposure time.

[0003]   Fig. 1 illustrates an imaging system 100 that performs digital CDS by subtracting the reset signal from the raw image signal for a pixel after the separate signals have been converted to digital values. Imaging system 100 includes a CMOS image sensor array 110 including rows and column pixel sensors, a row control circuit 120, sample-and-hold circuits 130, column select circuitry 140, an analog-to-digital converter 150, a digital data path 160, a reset buffer 170, and a digital processor 180.

[0004]   Row control circuit 120 can begin a digital CDS process in imaging sensor 100 by resetting a selected row of pixel sensors in CMOS sensor array 110. Sample-and-hold circuits 130 then immediately sample the reset voltages of the pixel sensors in the selected row. The reset voltages can then be sequentially converted to digital reset values, using column select circuit 140 to select individual sampled reset voltages and ADC 150 to convert the individual reset voltages into the digital reset values. The digital reset values can then be

saved in buffer 170 for later use.

[0005]   While the reset voltages are being converted to digital reset values, the selected row of pixel sensors discharge (or charge) the reset voltages at a rate that depends on the intensity of incident light on individual pixel sensors. At the end of an exposure time Texp, the pixel voltages, which were initially at the reset voltage levels, indicate the integrated light intensities over the exposure time Texp. Sample-and-hold circuits 130 then sample the integrated voltages of pixel sensors in the selected row, and column select circuit 140 and ADC 150 sequentially convert the integrated voltages to digital integrated values. Processor 180 can then determine the difference between the digital reset values in reset buffer 170 and the just determined the digital integrated values.

[0006]   Some potential drawbacks of digital CDS are frame rate reduction and timing changes during imaging. For each frame of corrected pixel data, separate output of digital integrated values and reset values doubles the data to flow through the analog channel (e.g., through ADC 150 in Fig. 1) when compared to imaging without digital CDS. In a worst case, serial output of twice the data can nearly double the time required to capture an image or frame.

[0007]   Fig. 2A illustrates the timing of an imaging process 200 without digital CDS. For imaging process 200, a first row of pixel sensors is reset at time T0 and begins integration of the incident light intensities on the pixel sensors. The integrated voltages for the first row are sampled at a time T0+Texp, where Texp is the exposure time, and a conversion and output process for the sampled integrated voltages for the first row of pixel sensors can commence. The integration process for the next row can begin at a time T1 that is selected so that integration for the row finishes when output of pixel values for the preceding row is complete. Accordingly, output of pixel values for the next row starts immediately after output of pixel values for the preceding row is complete. The total time Ttot required to output a frame of pixel data using the process of Fig. 2A is thus given by Equation (1) where Texp is the exposure time, Tout is the time required to output a row of digital data, and Nrow is the number of rows in the image sensor.

$$Ttot = Texp + Nrow*Tout \qquad (1)$$

[0008]   A conventional imaging device generally cannot implement the timing of Fig. 1 if the imaging device performs digital CDS. Fig. 2B illustrates the effect of resetting each row

at times T0, T1, and T2 that are the same described for Fig. 2A. In particular, reset times T1, T2, ... are selected to provide uninterrupted output of sample data from successive rows. Sampling and output of reset data begins when each row is reset, e.g., at times T0, T1, ..., and sample and output of integrated data occurs after the passage of exposure time Texp, e.g., at times T0+Texp, T1+exp, ... A conflict arises if the output of reset values overlaps the output of integrated values. Accordingly, output of digital reset values cannot be added to process 210 unless the exposure time is long enough that all reset values can be output before exposure of the first row is complete (i.e., Texp > Tout*(Nrow+1)).

[0009]   The timing of the imaging process for the conventional imaging device 100 must be altered to prevent output of reset data from conflicting with the output of raw pixel data. The alterations generally increase time required from output of data representing an image. In particular, the time required for an imaging process for a frame using digital CDS in imaging device 100 of Fig. 1, is greater than 2*Nrow*Tout and typically much greater than the time Texp + Nrow*Tout required for the imaging process 210 without digital CDS. Methods and systems that provide faster digital CDS processes and higher frame rates for shorter exposure times are thus desired.

SUMMARY

[0010]   In accordance with an aspect of the invention, an imaging sensor capable of performing digital correlated double sampling (CDS) includes two analog paths for parallel conversion of integrated voltages and reset voltages. Output of reset values and integrated values can thus overlap, and imaging can achieve a faster frame rate for high quality images.

[0011]   One specific embodiment of the invention is an imaging system that includes: an array of pixel sensors; a first bank of sample-and-hold circuits; a second bank of sample-and-hold circuits; a first analog-to-digital converter (ADC); a second ADC; and a selection circuit. Each bank of sample-and-hold circuits typically includes one sample-and-hold circuit per column of the sensor array. The selection circuit can select and connect a sample-and-hold circuit from the first bank to the first analog-to-digital converter while simultaneously selecting and connecting a sample-and-hold circuit from the second bank to the second analog-to-digital converter.

[0012]   A control circuit can activate the first bank to sample reset voltages in a selected

set (e.g., a row) of pixel sensors and activate the second bank to sample integrated voltages in a second selected set of pixel sensors. Accordingly, a digital reset value for one row of pixel sensors can be output simultaneously with output of a digital integrated value for another row of pixel sensors. The imaging system can further include a FIFO buffer coupled to receive a digital output signal from the first analog-to-digital converter. An adder can then determine a difference between a digital output signal from the FIFO buffer and a digital output signal from the second analog-to-digital converter to determine corrected pixel values.

[0013]   Another specific embodiment of the invention is an imaging method. The method includes: (a) resetting selected pixel sensors in an image sensor; (b) sampling reset voltages of the selected pixel sensors; (c) converting the reset voltages to digital reset values using a first channel; (d) sampling integrated voltage of the selected pixel sensors after lapse of an exposure time; (e) converting the integrated voltages to digital integrated values using a second channel; (f) changing which pixel sensors are selected; and (g) repeating steps (a) to (f). Converting the integrated voltages (e.g., for one row of a pixel sensor array) may overlap with converting the reset voltage (e.g., for another row of the pixel sensor array).

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]   Fig. 1 is a block diagram of a known imaging system.

[0015]   Fig. 2A is a timing diagram for a conventional imaging process without digital correlated double sampling.

[0016]   Fig. 2B is a timing diagram illustrating a potential data path conflict that results for an imaging process including digital correlated double sampling (CDS) and the same timing as the process of Fig. 2A.

[0017]   Fig. 3 is a block diagram of an imaging system in accordance with an embodiment of the invention.

[0018]   Fig. 4 is a timing diagram for an imaging process with digital CDS in the imaging system of Fig. 3.

[0019]   Fig. 5 is a timing diagram illustrating a process in accordance with an embodiment of the invention for capturing a series of images.

[0020]   Fig. 6 is a circuit diagram of a dual analog data path suitable for a high frame rate

-4-

imaging system with analog or digital correlated double sampling.

[0021]   Use of the same reference symbols in different figures indicates similar or identical items.

DETAILED DESCRIPTION

[0022]   In accordance with an aspect of the invention, an imaging system includes dual analog data paths that permit overlapping output of integrated values and reset values for digital correlated double sampling (CDS).

[0023]   Fig. 3 is a block diagram of an imaging system 300 in accordance with an exemplary embodiment of the invention. Imaging system 300 includes an array 110 of pixel sensors, a row control circuit 320, sample-and-hold circuits 330, column and channel select circuits 340, a pair of analog-to-digital converters (ADCs) 350 and 355, and an output control circuit 380.

[0024]   Sensor array 110 is an image sensor, which can be of a conventional design. In the exemplary embodiment of the invention, sensor array 110 is a CMOS image sensor including pixel sensors arranged in rows and columns. Each pixel sensor generally includes a capacitor connected to a photo-diode that charges or discharges the capacitor at a rate that depends on the intensity of light incident on the photodiode. A reset operation for a row of array 110 sets the capacitors in each pixel sensor in the row to a reset voltage level. A readout operation for a row of pixel sensors causes drive circuits in the pixel sensors of the selected row to drive column lines to voltage levels corresponding to the charge on the respective capacitors.

[0025]   Row control circuit 320 controls the timing of reset operations for the rows of pixel sensors in array 110 and selects which row of pixel sensors in array 110 drive the column lines of array 110. Such circuits for control of image sensor arrays are well-known in the art and can be of a conventional design.

[0026]   Sample-and-hold circuits 330 include two banks 331 and 332 that are connected to the column lines of sensor array 110. Each bank 331 or 332 contains one sample-and-hold circuit per column of pixel sensors in array 110. Output control circuit 380 can enable sample-and-hold circuits in bank 331 independently of the sample-and-hold circuits of bank

332. Accordingly, for each column of array 110, sample-and-hold circuits 330 can simultaneously hold two analog voltage levels (one in each bank) corresponding to the column line voltage at different times.

[0027] Select circuits 340 select and connect a sample-and-hold circuit in bank 331 to ADC 350 and/or a sample-and-hold circuit in bank 332 to ADC 355. ADCs 350 and 355 convert the sampled analog voltages from sample-and-hold circuits 331 and 332 to digital values. As a result, two digital values, one from ADC 350 and one from ADC 355, can be simultaneously output. In one operating mode of imaging system 300, ADC 350 is selected for output of digital reset values and is connected to a FIFO buffer 360, and ADC 355 is selected for output of raw integrated values and is connected to an adder 370. For digital CDS, adder 370 determines a difference between the raw integrated value currently output from ADC 355 and a reset value in FIFO buffer 360.

[0028] Fig. 4 illustrates the timing of an imaging process 400 with digital CDS in imaging system 300 of Fig. 3. Imaging process 400 starts at time T0, when row control circuit 320 causes sensor array 110 to reset the pixel sensors in row 0. Bank 331 of the sample-and-hold circuits 330 immediately samples the reset voltages of row 0 through appropriate column lines, and an output process 402 for the reset values begins using ADC 350 to sequentially convert the analog reset voltages from the pixel sensors in row 0 to digital reset values stored in FIFO buffer 360.

[0029] An integration process 404 in the pixel sensors of row 0 begins immediately after sampling of the reset voltages, causing the voltages in the pixel sensors in row 0 to change at rates that depend on respective light intensities incident on the pixel sensors. Output and sampling of the integrated voltages from the pixel sensors in row 0 occurs after passage of exposure time Texp (i.e., at a time T0+Texp) when integration process 404 is complete. Bank 332 then samples the integrated voltages, and an output process 406 through ADC 355 begins.

[0030] A reset operation for row 1 occurs at a time T1. The time interval between time T1 and time T0 is about equal to the time Tout required to complete the output process for a row of pixel values, so that an output process 412 for reset values for row 1 begins through ADC 350, immediately after output process 402 for row 0 ends. Accordingly, output processes 402 and 412, which use the same analog channel through ADC 350, efficiently use

ADC 350 to maximize the data output rate without data conflicts.

[0031]   An output process 416 of integrated values for row 1 begins at a time T1+Texp, which is after an integration operation 414 is complete. Since time T1 follows time T0 by row output time Tout, output process 416 begins at time T0+Texp+Ttot, which is immediately after the output process 406 for row 0 ends. Accordingly, the output processes 406 and 416 through ADC 355 provide continuous data output and do not conflict.

[0032]   Operations for succeeding rows (e.g., output operation 422 for reset values of row 2, integration operation 424, and output operation 426 for integrated values of row 2) follow respective operations for the prior row (e.g., operations 412, 414, and 416 for row 1) by output time Ttot. Accordingly, ADC 350 provides continuous output of one digital reset value per clock cycle beginning with the first digital reset value for an image, and ADC 355 provides continuous output of one digital integrated value per clock cycle beginning with the first digital integrated value for the image. The start of the stream of digital integrated values for the image follows the start of the stream of the digital reset values for the frame by lapse of the exposure time Texp.

[0033]   Fig. 4 illustrates the case where exposure time Texp is about twice the output time Ttot for a row of digital values. In this case, output operation 406 for the integrated values from row 0 occurs at about the same time as output operation 422 for the reset values form row 2. However, no data path conflict occurs since the reset and integrated values are output through separate analog data paths. More generally, the timing of the output processes 402, 412, ... for the reset values relative to the output processes 406, 416, ... for the integrated values depends on the exposure time Texp, but the same output process can be efficiently used for all exposure times Texp regardless of whether the exposure time is greater or less than Nrow*Tout. The time required for imaging process 400 is Texp+Nrow*Tout, the same as the time required for a conventional imaging process 200 given in Equation (1).

[0034]   FIFO buffer 360 has a capacity to hold at least the number of reset values that are output during the exposure time Texp or a maximum of one full frame of reset values. In the illustrated example of Fig. 4, exposure time Texp is about twice the output time Tout for a row of values, and FIFO buffer 360 must be able to store at least two rows of reset values. Output reset values from FIFO 360 automatically correspond to the same pixel as the integrated values in imaging process 400 when the integrated values (e.g., in processes 406,

416, ...) are output in the same order as reset values (in processes 402, 412, ...).

[0035]   Digital CDS imaging processes using dual analog channels for successive frames or images can be overlapped to increase the effective frame rate. Fig. 5 illustrates the timing for a process 500 capturing a series of frames forming a moving image. The imaging process for a first frame (frame 1) is conducted in the manner of imaging process 400 of Fig. 4. In particular, an output process 510 through a first analog channel begins at the start of the imaging process for frame 1, and an output process 515 through a second analog channel begins after lapse of the exposure time Texp. As noted above, output process 510 is for digital values representing the reset voltages of the pixel sensors of the image array, and output process 520 is for digital values representing the integrated voltages from the pixel sensors. The time required for each process 510 or 515 is the product of the number of row Nrow in the image sensor array, and the output time Tout for a row of pixel sensors.

[0036]   An output process 520 for reset values used in a second frame (frame 2) can begin right after process 510 is complete. Accordingly, output process 520 of reset values for frame 2 overlaps output process 515 for integrated values of frame 1. The overlap time is equal to the exposure time Texp. Accordingly, if the exposure time Texp is less than the total time Nrow*Tout required to output digital values for the entire image sensor array, the frame rate for long series of frames will be about 1/(Nrow*Tout). In contrast, if imaging processes for successive frames are not overlapped, the frame rate would be lower, i.e., 1/(Texp+Nrow*Tout), which can be a significantly lower frame rate when the exposure time Texp is large.

[0037]   Fig. 6 illustrates a portion of an image sensor output circuit 600 in accordance with an embodiment of the invention providing dual analog channels for output of image data. Output circuit 600 includes sample-and-hold circuits 610 and 615, mode select circuits 620, column select circuits 630, pixel reset output buses 641 and 642, pixel exposed output buses 643 and 644, and analog-to-digital converters 650 and 655.

[0038]   Sample-and-hold circuits 610 and 615 are connected to column lines of an image sensor (not shown). Each column of pixel sensors in the image sensor array has one sample-and-hold circuit 610 and one sample-and-hold circuit 615, but for ease of illustration, Fig. 6 shows only the circuits 610 and 615 for two columns of pixel sensors. Sample-and-hold circuits 610 and 615 operate separately and can be triggered at different times to sample the

analog voltages on respective column lines.

[0039]   Mode select circuits 620 and column select circuits 630 connect the sample-and-hold circuits 610 and 615 for a selected column (or selected columns) to analog output buses 641 to 644, which provide input signals to ADCs 650 and 655. Mode select circuits 620 can select among a digital correlated double sampling mode and two analog correlated double sampling modes depending on the signal levels of signals DCDS, A0A, A0B, A1A, and A1B. Column select circuits 630 select a column of pixel sensors for data output.

[0040]   Column select circuits 630 sequentially enable mode select circuits 620 in response to column select signals COLSEL0, COLSEL1, ... from column control circuitry (not shown). In an exemplary embodiment, mode select circuits 620 are sequentially enabled for sequential conversion of sampled voltages to digital values.

[0041]   Signal DCDS is asserted for digital correlated double sampling. When signal DCDS is asserted, the enabled mode select circuit 620 connects the analog output from the corresponding sample-and-hold circuit 610 to pixel reset bus 642 and connects the analog output from the corresponding sample-and-hold circuit 615 to pixel exposed bus 644. A reference device 625 simultaneously charges buses 641 and 643 to a reference voltage Vref. ADC 650 converts a voltage difference between reference voltage Vref and the sampled reset voltage from the sample-and-hold circuit 610 for the selected column to a digital reset value. ADC 655 simultaneously converts a voltage difference between reference voltage Vref and the sampled integrated voltage from the sample-and-hold circuit 615 for the selected column to a digital integrated value.

[0042]   To implement the imaging process 400 of Fig. 4, row 0 is reset at time T0, and sample-and-hold circuits 610 in circuit 600 sample the reset voltages. Output process 402 then begins through sequential activation of column select signals COLSEL0, COLSEL1, etc. Reset values from ADC 650 can be stored in a FIFO buffer (not shown). If the reset values correspond to a single image or the first image of a series, the integrated values from ADC 655 are ignored. However, for a second or subsequent frame in a moving image, the integrated values output from ADC 655 correspond to the preceding frame when ADC 650 outputs reset values for row 0.

[0043]   The readout process of reset values for the current frame continues until, the FIFO buffer contains a number of reset values for the current frame corresponding to the exposure

time Texp. At that time Texp, sample-and-hold circuits 615 sample the integrated voltages from row 0 of the image sensor array, and ADC 655 begins output of the digital integrated values for row 0, while ADC 650 outputs digital reset values for another for, e.g., row (Texp/Tout − 1). Corrected pixel values are generated from the differences of the integrated values currently output and the stored reset values from the FIFO buffer.

[0044]   Output circuit 600 can also implant analog CDS. Signal A0A, A0B, A1A, and A1B are used to select among different analog CDS modes that use one or both analog data paths. Signals A0A and A1A are asserted for analog CDS using only the analog data path to ADC 650. For this analog CDS mode, a row is reset, and sample-and-hold circuits 610 sample the reset voltages. After the exposure time, sample-and-hold circuits 615 sample the integrated voltages, and a conversion and output process begins. For the output process, the enabled mode select circuit 630 for the selected column connects the corresponding sample-and-hold circuit 610 to bus 641 and connects the corresponding sample-and-hold circuit 615 to bus 642. ADC 650 converts the voltage difference the sampled reset voltage and the sampled integrated voltage into a digital pixel value.

[0045]   After the digital pixel values for a row are generated, the next row is reset and sampled, and integration begins. The operations of successive rows are not overlapped. Accordingly, the time required to generate a frame of pixel data is about Nrow*(Texp+Tout).

[0046]   Signals A0B and A1B are asserted for a similar analog CDS using only the analog data path through ADC 655. However, ADC 650 and 655 can be used in parallel to cut the output time Tout in half. For example, if signals A0A and A1B are asserted, and a pair of column select signals (e.g., COLSEL0 and COLSEL1) are simultaneously asserted, two pixel values are output at a time, and output time Tout is cut in half.

[0047]   Although the invention has been described with reference to particular embodiments, the description is only an example of the invention's application and should not be taken as a limitation. Various adaptations and combinations of features of the embodiments disclosed are within the scope of the invention as defined by the following claims.